In the Claims:

Please amend claim 1 as indicated below:

1.(Currently Amended) A digital imaging system comprising:

an image sensor;

image processing and compression circuits; and

~~an~~ a high density analog/multi-level memory coupled between said image sensor and said image processing and compression circuits to receive and temporarily store analog data from said image sensor and transmit said analog data to said image processing and compression circuits.

Please present claims 13 with the indentation as indicated below:

13.(Re-presented (altered indentation)) The system of Claim 2, wherein said memory comprises:

a plurality of write pipelines, each write pipeline comprising:

an array of non-volatile memory cells; and

a write circuit coupled to the array, wherein when started on a programming operation for a selected memory cell in the array, the write circuit applies a first voltage to the selected memory cell to drive a current through the selected memory cell;

a timing circuit coupled to sequentially start programming operations by the write circuits; and

a charge pump that generates the first voltage from a supply voltage and is coupled to the write circuits to supply the first voltage for the programming operations.

Please amend claims 15-17 as indicated below:

15.(Currently Amended) ~~The~~ A digital imaging system ~~of Claim 13~~ comprising:

an image sensor;

image processing and compression circuits; and

an analog/multi-level memory coupled between said image sensor and said image processing and compression circuits to receive and temporarily store analog data from said image sensor and transmit said analog data to said image processing and compression

circuits, wherein said memory receives said data at a rate of greater than 10 Mbits/sec for more than 5 seconds and stores more than 50 Mbits of said data and, wherein said memory comprises:

a plurality of write pipelines each write pipeline comprising:

an array of non-volatile memory cells; and

a write circuit coupled to the array, wherein when started on a programming operation for a selected memory cell in the array, the write circuit applies a first voltage to the selected memory cell to drive a current through the selected memory cell;

a timing circuit coupled to sequentially start programming operations by the write circuits; and

a charge pump that generates the first voltage from a supply voltage and is coupled to the write circuits to supply the first voltage for the programming operations, and

wherein the write pipelines comprise:

a plurality of odd numbered pipelines; and

a plurality of even numbered pipelines,

wherein when an odd numbered pipeline and an even numbered pipeline are both performing programming operations, a selection circuit in the odd numbered pipeline selects the first voltage when ~~the~~ a selection circuit in the even numbered pipeline selects ~~the~~ a second voltage and a selection circuit in the odd numbered pipeline selects the second voltage when the selection circuit in the even numbered pipeline selects the first voltage.

16.(Currently Amended) The system of Claim 2, wherein said memory comprises:

a plurality of banks of write pipelines, each write pipeline comprising:

an array of non-volatile memory cells; and

a write circuit coupled to the array, wherein:

during a programming cycle for a selected memory cell in the array, the write circuit applies a first voltage to drive a current through the selected memory cell and change ~~the~~ a threshold voltage of the selected

memory cell; and

during a verify cycle for the selected memory cell, the write circuit determines whether a threshold voltage of the selected memory cell has reached a target level representing a value being written into the selected memory cell;

a charge pump that generates the first voltage from a supply voltage and is coupled to the write circuits to supply the first voltage for the programming cycles; and

a timing circuit coupled to start programming cycles in the pipelines, wherein the timing circuit starts programming cycles for each bank at times that are different from when programming cycles start in the other banks.

17.(Currently Amended) The system of Claim 16, wherein the plurality of banks comprises a first bank and a second bank, and the ~~time~~ timing circuit starts programming cycles in the first bank when verify cycles start in the second bank.

Please add the following new claims:

--24.(New) A digital imaging system comprising:

an image sensor;

image processing and compression circuits; and

an analog/multi-level memory coupled between said image sensor and said image processing and compression circuits to receive and temporarily store analog data from said image sensor and transmit said analog data to said image processing and compression circuits, wherein said memory comprises:

a plurality of odd numbered write pipelines and a plurality of even numbered write pipelines, each write pipeline comprising:

an array of non-volatile memory cells; and

a write circuit coupled to the array, wherein when started on a programming operation for a selected memory cell in the array, the write circuit applies a first voltage to the selected memory cell to drive a current through the selected memory cell, wherein when an odd numbered pipeline and an even numbered pipeline are both performing programming operations, a selection circuit in the odd numbered pipeline selects the first voltage when a

selection circuit in the even numbered pipeline selects a second voltage and a selection circuit in the odd numbered pipeline selects the second voltage when the selection circuit in the even numbered pipeline selects the first voltage.

25.(New) The system of Claim 1, wherein said stored analog data is externally accessible.

26.(New) The method of Claim 18, further comprising:
accessing said stored analog data in analog form prior to said transmitting.--